Nobel Implementation of a Line Driver

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Abstract— Purpose of this paper is to describe the hardware design implementation of Line Driver. Line driver provides an economic solution to extend DTE interfaces over 2 copper wires up to 5.5 km. This provides adaptive echo cancellation to get high quality 64 Kbps/128Kbps digital data transport. This is equipped with one DTE data port which can be selected to run at 64 to 128 Kbps speed synchronously and this is designed to work over telephone lines. This line driver has lightning protection circuit and can withstand AC. This line driver features extensive diagnostics menu to assist installers and operators to troubleshoot line problem. This offers payload loop back and DTE to DTE loop back.

Index Terms— DTE, G.703, LAN, ROUTER,V.35,

1 Introduction

The Line Driver is a full duplex 64/128 Kbps used for data Transmission over 2-wire unconditioned twisted copper pairs. This provides Point-to-Point Digital Connectivity over leased lines through telecommunication network or privately owned circuits to interconnect the workstations or networking equipment located at two different places.

2 Application of Line Driver

The line driver can be used as a high speed base band modem that connects two DTEs over a leased line.

2.1 64Kbps G.703 to V.35 wide area point to point connectivity

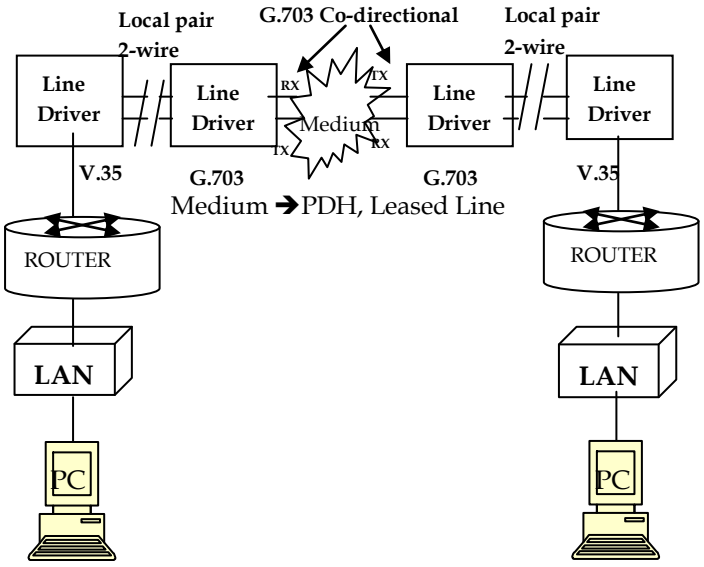

Fig.1. 64Kbps G.703 to V.35 wide area point to point connectivity

2.2 64 Kbps G.703 to Async wide area point to point connectivity

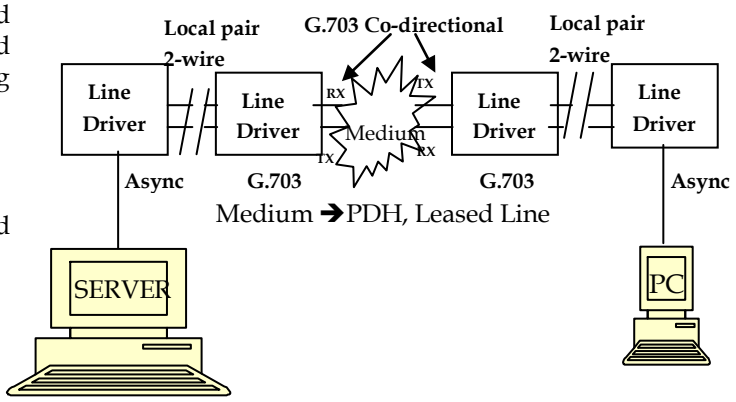

Fig.2. 64Kbps G.703 to Asynchrounous wide area point to point connectivity

2.3 64Kbps G.703 to Ethernet wide area point to point connectivity

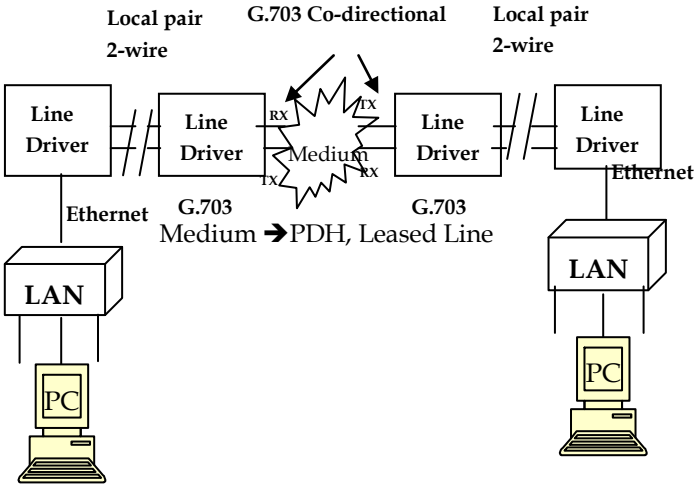

Fig.3. 64Kbps G.703 to Ethernet wide area point to point connectivity

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3 SYSTEM SPECIFICATION

3.1 LINE INTERFACE

Type: full duplex adaptive echo cancellation; line coding: 2B1Q; Line type: Unconditioned twisted pair 19-26 AWG; connector: RJ45.

3.2 USER INTERFACE OPTION

3.2.1 DTE INTERFACE(V.35)

Interface: V.35; connector: M34; data rate: 64Kbps or 128 Kbps synchronous
V.35/M34 DTE port definition

Pin no.	signal	source
A	Cable Shield	
B	Signal Ground	
C	Request to send	DTE
D	Clear To Send	DCE
E	Data set ready	DCE
F	Data Carrier Detect	DCE
H	DataTerminal Ready	DTE
J	Unassigned	
K	Unassigned	
L	Unassigned	
M	Unassigned	
N	Unassigned	
P	Transmit Data	DTE
R	Receive Data	DCE
S	TransmitDataReturn	DTE
T	Receive Data Return	DCE
U	External Clock	DTE
V	Receive Clock	DCE
W	External clock Return	DTE
X	Receive Clock Return	DCE
Y	Transmit Clock	DCE
Z	Unassigned	
AA	Transmit Clock Return	DCE
BB	Unassigned	
CC	Unassigned	
DD	Unassigned	
EE	Unassigned	
FF	Unassigned	
HH	Unassigned	
JJ	Unassigned	
KK	Unassigned	
LL	Unassigned	
MM	Unassigned	
NN	Unassigned	

Table1: V.35/M34 DTE port definition

3.2.2 CO-DIRECTIONAL INTERFACE

Interface: ITU G.703 64Kbps co-directional interface; connector: 120ohm, RJ48; loop back: DTE payload loop back, DTE to Line Loop back.
G.703 64Kbps pin assignment (RJ48)

Pin number	signal
1	Receive Ring
2	Receive Tip
3	Unassigned
4	Transmit Ring
5	Transmit Tip
6	Unassigned
7	Unassigned
8	Unassigned

Table2: RJ48 pin assignment

3.3 CLOCK SOURCE

Internal, Line or DTE.

3.4 DIAGNOGSTICS TEST

Local loop on CPE, remote loop on CPE, local loop on network, remote loop on network.

3.5 FRONT PANEL INDICATIONS

Front panel LED indicators will be there to indicate different status-Power, line Sync, line Test, DTE test, DTE transmit data (TD), DTE receive data (RD),DTE clock loss(clk loss).

3.5 VOLTAGE AND POWER REQUIREMENTS

U-interface chip[1] will require +5V and 1watt (max.). G.703 interface chip will require +5V and 1watt (max.).V.35 interface chip will require +5V and 1watt (max.).FPGA will require 1.2V, 2.5V, 3.3V and 1watt (max.).Microcontroller and its peripheral will require 5V and 1watt (max.).

4 SIMPLIFIED INTERNAL BLOCK DIAGRAM

U-interface chip[1] is configured by microcontroller or by FPGA. The 2Mbps, 1 TS and TX and RX clock are connected to FPGA.The U-interface is connected to two wire copper wire via 4 -wires to 2 wire bridge circuit. This chip transmits the 2B1Q data format through the line. This line is connected to RJ48 connector.
The XR-T6166 [2] and the companion XR-T6164 [3] line interface chip together form a CCITT G.703 compliant 64 kbps co-directional interface. The XR-T6166 [2] contains separate transmit and receive sections. The transmitter transforms 8 bit serial data from 2.048 Mbps time slot into an encoded 64 kbps data stream.The receiver which conforms the reverse opera-

tion, decodes the 64 kbps data, extracts a clock signal and then outputs the data to 2.048 mbps time slot. The XRT6164 is a general purpose line interface chip that contains the receive and transmit circuitry necessary to convert TTL logic levels to a bipolar signal both to and from a twisted pair cable.
The XRT6164 receiver section converts a balanced bipolar signal that has been attenuated and distorted by up to 10 dB of twisted pair cable to active-low TTL compatible logic levels. The XRT6164 transmitter section contains two matched open collector output drivers that are capable of driving the line transformer directly with a current up to 40 mA. The transmitter digital inputs which are active high are TTL compatible. V.35 uses differential interfaces for the clock and data signals which the only signals are requiring high switching speeds for high-speed communications.Basically V.35 is a high speed serial interface desgned to support both higher data rates and connectivity between DTEs(data terminal equipment) or DCE(data communication equipment) over digital lines. FPGA [4] is used to control the entire front panel LEDs (indicator). 8 KHz, 2Mbps and gaper clock are supplied from FPGA.FIFO may be defined in FAGA.

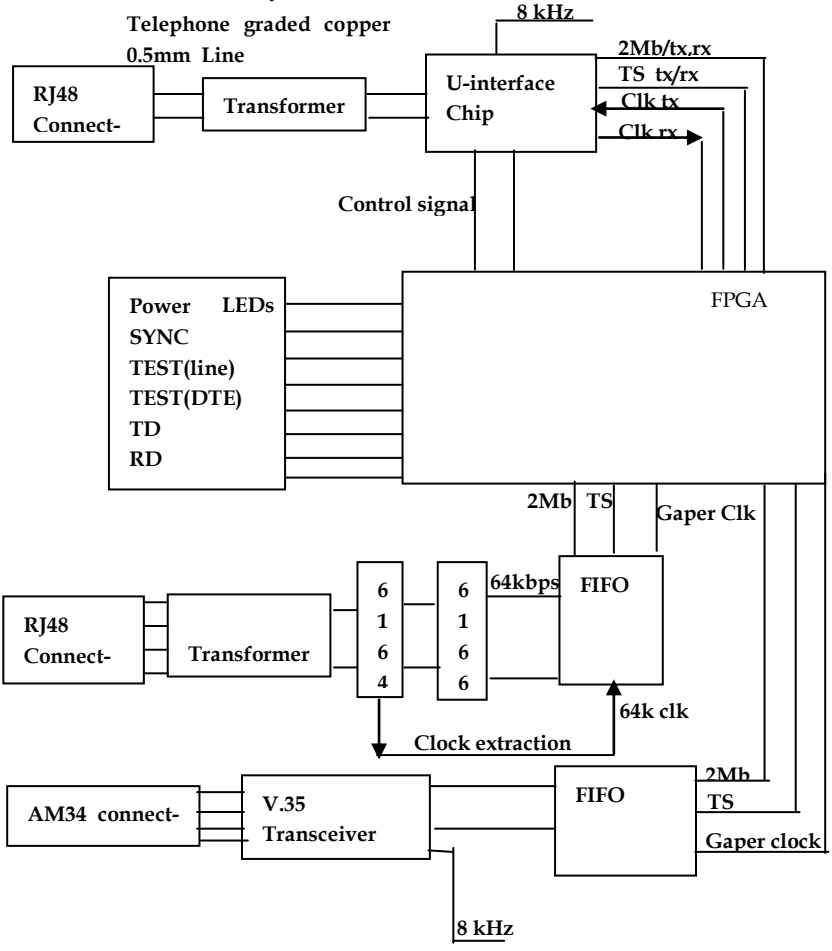

Fig4. Internal Block diagram of line driver

5 NEAR END LOOP BACK

The out going is looped back through U interface transceiver.

All 128K data are looped back to the receiver path. This loop back test is activated by a Test command. Payload loop back is illustrated in the following figure. The incoming signal is loop back to the outgoing U transmitter after the U receiver. This loop back is used to isolate the DTE ports from the troubled U interface line.DTE to DTE port loop back is illustrated in the following figure. TO-DTE is when DTE incoming signal is loop back to the DTE outgoing signal. This loop back is used to validate the unit integrity of DTE facility.

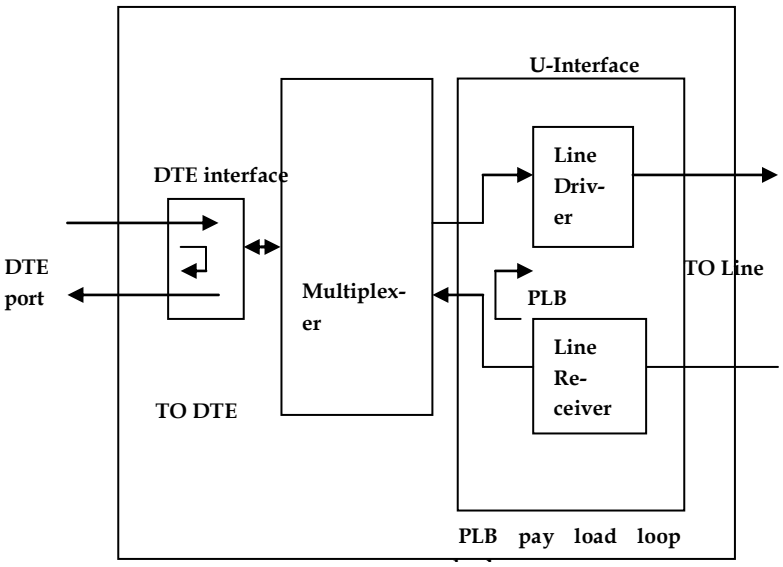

Fig5. Near end loop back

6 CONCLUSION

After calculating individual cost of components the total Cost of this line driver is near about $40.The overall power consumption is about 5 watt.

REFERENCES

[1] Data sheets of "MC145472 U-interface transceiver" by Motorola.

[2] Data sheets of "XRT-6166 co-directional digital data processor"by EXAR.

[3] Data sheets of "XRT-6164 Digital line interface tranceiver"by EXAR.

[4] Data sheets of "EPF10K10- Embedded Programmable Logic Device Family" by ALTERA.